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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/662,358	09/15/2000	Taiji Noda	0819-0423	1724

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EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 02/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/662,358	NODA ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 02 December 2003.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-10,12-15 and 21-24 is/are pending in the application.

4a) Of the above claim(s) 1-5 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 6-10,12-15 and 21-24 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

1. Amendment filed December 2, 2003 has been entered. Claims 6 and 7 20 have been amended. canceled. Claims 1-10,12-15 and 21-24 are pending. Claims 1-5 have been withdrawn.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 6-10, 12-14 and 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over G.G. Shahidi et al., *High-Performance Devices for a 0.15 μm CMOS Technology*, in view of Burr (U.S. Patent No. 5,923,987) all of record.

With respect to claim 6, Shahidi teaches a method for fabricating a semiconductor device substantially as claimed including:

a first step of forming a gate electrode over a semiconductor region with a gate insulating film interposed therebetween;

a second step of implanting heavy ions (In) into the semiconductor region on both side of the gate electrode using the gate electrode as a mask, thereby forming a first (In) ion implanted layer of the second conductivity type (p), at least upper part of which is an amorphous layer; and

a third step of implanting ions (As) of a first dopant into the semiconductor region, in which the amorphous layer has been formed, using the gate electrode as a mask, thereby forming a second (As) ion implanted layer of the first conductivity type (n). (See page 466-468).

Thus, Shahidi is shown to teach all the features of the claim with the exception of explicitly disclosing an anneal process to activate the first and second implanted dopants.

However, Burr teaches following the implantations of the first (347) and second (336) implanted layers, it is generally required conducting a first annealing process to activate the first (347) and second (336) ion implanted layers, thereby forming the extended high-concentration dopant diffused layer (336) of the first conductivity type (n) through diffusion of the first dopant and the pocket dopant diffused layer (347) of the second conductivity type (p), which is in contact with bottom portion of the extended high-concentration dopant diffused layer (336), through diffusion of the heavy ions (347), respectively. (See Fig. 5H, col. 15, ll. 1-9).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to conduct a first annealing process to activate the first (In) and second (As) implanted dopants of Shahidi as taught by Burr because the process step is required and is well known in the art. (See col. 15, lines 1-9).

With respect to the term "wherein in the second step, a dislocation loop layer is formed in the lower region of the amorphous layer in the semiconductor region due to the heavy ions implantation", the formation of dislocation loop is an inherent result of implantation using heavy ions such as indium.

With respect to the term "in the fourth step, the pocket dopant diffused layer including a part in which the heavy ions are trapped is formed in the dislocation loop layer", again, this

formation is an inherent result of anneal activation following the implantation of heavy ions, since Shahidi, in view of Burr has performed all process steps as claimed.

With respect to claim 7, since Shahidi, in view of Burr, performs all process steps as claimed the part of the pocket dopant (In) diffused layer of Shahidi in which the heavy ions are trapped should overlap with a dopant profile of the extended high-concentration dopant (As) diffused layer. Also see Burr, Fig. 5H.

Note that, the dislocation loop layer is locate at a level deeper than the peak concentration of the heavy ions in the substrate.

With respect to claim 8, method of Shahidi in view of Burr further includes:

forming a sidewall spacer (335) on side faces of the gate electrode (342) after the third step has been performed;

implanting ions of a second dopant (n^+) into the semiconductor region using the gate electrode (342) and the sidewall spacer (335) as a mask, thereby forming a third ion implanted layer (336/338) of the first conductivity type (n); and

conducting a second annealing process to activate the third ion implanted layer, thereby forming a high-concentration dopant diffused layer of the first conductivity type, which is located outside of the extended high-concentration dopant diffused layer (336A), has a junction deeper than that of the extended high-concentration dopant diffused layer (336A) and has been formed through diffusion of a second dopant. (See Fig. 5I).

With respect to claim 9, the heavy ions (In) of Shahidi are implanted at such an implant energy as forming an amorphous crystalline interface, through implantation of the heavy ions (In), at a level equal to or deeper than a range of the first dopant and shallower than a range of the second dopant.

With respect to claim 10, method of Shahidi in view of Burr further includes:

implanting ions (p) into a surface part of the semiconductor region, thereby forming a fourth ion implanted (channel) layer of a second conductivity type (p) before the first step is performed; and

conducting a third annealing process to activate the fourth ion implanted layer, thereby forming a dopant diffused layer (334) to be a channel region. (Also see Fig. 5B).

With respect to claim 12, the heavy ions (In) of Shahidi are implanted at such an implant energy as getting a range of the heavy ions (In) equal to or deeper than a range of the first dopant (As) and between one to three times as deep as the range of the first dopant (As).

With respect to claim 13, the heavy ions of Shahidi and Burr includes indium ions.

With respect to claim 14, the implant dose of the heavy ions of Shahidi in view of Burr is within the order of magnitude as claimed.

Further, within purview of one having ordinary skill in the art, it would have been obvious to determine the optimum dose of the ions implanted. See In re Aller, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation".

With respect to claim 21, the first dopant of Shahidi and Burr is arsenic.

With respect to claim 22, the heavy ions of Shahidi and Burr are indium ions.

With respect to claim 23, the heavy ions and the first dopant of Shahidi are indium ions and arsenic and the second dopant, in view of Burr '987, are arsenic.

With respect to claim 24, the fourth ion implanted layer of Shahidi id formed into the surface part of the semiconductor region by implanting indiums ions.

3. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shahidi et al. and Burr '987 as applied to claim 6 above, and further in view of Tsukamoto (U.S. Patent No. 5,399,506) (of record).

Shahidi and Burr '987 teach conducting the first annealing process using a rapid thermal annealing (RTA) as is well known to those skill in the art.

Thus, Shahidi and Burr '987 are shown to teach all the features of the claim with the exception of explicitly disclosing the details of RTA process.

However, Tsukamoto teaches that RTA process is well known in the art including: a semiconductor region is heated up to a temperature between 950 °C and 1050 °C at a rate between 100 °C/sec to 150 °C/sec and then kept at the temperature for a period of time between 1 to 10 seconds.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention perform the RTA process of Shahidi and Burr as taught by Tsukamoto to activate the dopants.

Further, within purview of one having ordinary skill in the art, it would have been obvious to determine the optimum annealing temperature and the temperature rate of increase to activate the dopant. See In re Aller, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation".

Response to Arguments

4. Applicant's arguments filed June 18, 2003 have been fully considered but they are not persuasive.

With respect to claim 6, Applicants argue that Shahidi fails to disclose a pocket dopant diffused layer including a part of the dislocation loop layer in which indium ions are trapped.

However, this characteristic of is an inherent result of implantation of heavy ions, wherein the dislocation loop layer formed at a level deeper than the peak concentration of ions implanted. Further, the implantation steps of Shahidi is similar to that of claimed invention, a similar dislocation loop and trapped should similarly occur.

With respect to Burr, Applicants contend: Burr fails to disclose forming an amorphous layer in the upper part of the pocket region (347) by ion implanting p-type ions or forming a dislocation loop layer. Hence, Burr fails to teach or suggest that, after the heat treatment, the pocket dopant diffused layer (347) includes a part of a dislocation loop layer would not be formed.

Note that, by implanting heavy ions such as indium, amorphization of the upper part of a substrate is an inherent result as well as the formation of dislocation loop layer.

Regarding the "trapped", a similar result as that of Shahidi, as discussed above, should also form following the anneal of the implanted substrate.

Applicants also state: in addition, as disclosed in lines 38-55 of column 14 of Burr the implanted dosage of the pocket region (347) is between $5x10^{11}$ and $1x10^{13}$ cm^{-2}. With such a range of dosage, even if indium ions are being implanted, an amorphous layer and a dislocation loop layer would not be formed.

Note that, "$1x10^{13}$ cm^{-2}" is clearly within the order of magnitude of the claimed dose "$5x10^{13}$ cm^{-2}". Applicant fails to provide any evidence to support his conclusion that "a dislocation loop layer would not be formed" at the dose of Burr.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 9:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A.M
January 29, 2004

LONG PHAM
PR[illegible] EXAMINER